Amendments to the Specification:

Please replace paragraph [0005] with the following amended paragraph:

[0005] Since the digital processing system stores data byte by byte, the 5 sets of bit data in columns 101~105 should be properly shifted and operated to be successfully accessed. For example,

Bit data in column 101 = data byte B11 & 0x0F;

Bit data in column 102 = ((data byte B12 & 0x03) << 4) | ((data byte B11 & 0xF0) >> 4);

Bit data in column 103 = ((data byte B13 & 0x01) << 6) | ((data byte B12 & 0xFC) >> 2);

Bit data in column 104 = (data byte B13 & 0x06) >> 1; and

Bit data in column 105 = (data byte B13 & 0xF8) >> 3;

wherein each of the expressions "0x0F", "0x03", "0xF0", "0x01", "0xFC", "0x06" and "0xF8" indicates an 8-bit hexadecimal mask data, the expression "X & Y" indicates an AND gate logic operation of X with Y, the expression "X | Y" indicates an OR gate logic operation of X with Y, the expression "X >> Y" indicates the rightward shift of the data X by Y ~~data units~~ bits, and the expression "X << Y" indicates the leftward shift of the data X by Y ~~data units~~ bits.

Please replace paragraphs [0051] and [0052] with the following amended paragraphs:

[0051] First of all, the bit number n is compared with the bit number m. Since n is greater than m in this example, the second clear and writing operation is performed. In other words, the masking procedure based on the mask data MD2 is performed first to clear the bits ~~except the bits~~ at the addresses (3)~(7) of the data storage zone 30, and the first byte R31 to be written into the data storage zone 30 is processed by a leftward shift operation L2 to be shifted by the amount of 3 bits, thereby obtaining an intermediate byte T31. The intermediate byte T31 is then written

into the data storage zone 30 at the addresses (3)~(7) as data byte B31 via a ~~wiring~~ writing procedure.

[0052] Further refer to Fig. 6B. Since the second byte R32 is the last byte to be written, the third clear and writing procedure is performed. In other words, the masking procedure based on the mask data MD3 is performed first to clear the bits ~~except the bits~~ at the addresses (8)~(12) ~~first~~ of the data storage zone 30. Then, the first byte R31 is processed by a rightward shift operation R2 to be shifted by the amount of 5 bits, and the second byte R32 is processed by a leftward shift operation L2 to be shifted by the amount of 3 bits to result in intermediate bytes T32 and T33. The bytes T32 and the bytes T33 are then synthesized via an OR gate operation to obtain a data byte T34. The intermediate byte T34 is then written into the data storage zone 30 at the addresses (8)~(12) as data byte B32 via a ~~wiring~~ writing procedure.